

Docket No.: PU020290
Customer No. 24498

Application No.: 10/518,278
Art Unit: 2619

Remarks/Arguments

Introduction

The Office Action mailed on November 21, 2007 has been reviewed and carefully considered.

Claims 1-16 are pending in this application.

Reconsideration of the above-identified application, as herein amended and in view of the following remarks, is respectfully requested.

As discussed herein below, the Applicant respectfully submits that the prior art references cited by the Examiner fail to disclose at least some features of the present claims.

Drawing Confirmation

Initially, applicant has notices that the publication No. 2005/0226211 corresponding to the subject application (Serial No. 10/518,278) only includes two (2) sheets of drawings for Figures 1 and 2, and seems to be missing Figure 3 which is clearly of record in the present application. Applicant respectfully requests that the Examiner confirm that Figure 3 is in the file as it was originally disclosed in the application.

Claim Rejections

Claims 1, 2, and 11 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Shuholm (U.S. Patent No. 6,104,997) (hereinafter 'Shuholm') in view of Cooper et al (U.S. Patent No. 5,550,594) (hereinafter "Cooper") and Watanabe et al. (U.S. Pub. 2002/0031148) (hereinafter Watanabe).

Initially, applicant would like to point out that Shuholm is a digital audio receiver with multi channel swapping capability which receives at least two input AES audio streams. The streams are decoded and each audio channel is stored in a separate buffer. The outputs of the buffers are input to at least two selectors which are under user control. The recombined digital audio streams are then input into a conventional router cross-point matrix for directing to a desired destination and formatted into new AES serial digital audio streams.

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However, Shuholm does not disclose or suggest a broadcast router as set forth by the present invention. A broadcast router is different from what many others call routers or switches in that a single input can feed any or all of the outputs simultaneously. Other types of routers, especially for example, those used in telecommunications can feed only one output from a given input. In the router 100 of the applicant's specification, the inputs and outputs are digital audio streams carrying two audio channels each.

As discussed in applicant's previous response, Shuholm discloses a digital audio receiver that is adapted to receive two digital audio streams at two decoder inputs (see, e.g., Shuholm, elements 12 and 13, Fig. 4; column 2, lines 30-34). Each stream includes multiple channels carrying digital audio and clock information, which are extracted from the streams by the decoders (see, e.g., Shuholm, column 2, lines 31-32). The clock data is used to write audio information from each channel to first-in first-out (FIFO) modules (see, e.g., Shuholm, column 2, lines 34-38). Under the control of system clocks, the audio data from each channel is transmitted to selectors, which are configured to output two digital audio streams that may include different combinations of audio channels originally received at the decoders (see, e.g., Shuholm, column 2, lines 39-48).

Although Shuholm discloses manipulation and switching of audio channels, Shuholm fails, as admitted by the Examiner, to disclose or render obvious employing a reference signal in lieu of another reference signal. A reference signal is well-known in the art and often times is utilized for timing purposes, including signal synchronization and timing switches within a broadcast router. Shuholm does not disclose switching of any reference signals. As stated above, the selector of Shuholm merely switches channels carrying audio data. While Shuholm employs clock data to write and output audio streams from the FIFO modules, nowhere does Shuholm disclose or suggest switching clock data extracted from the digital audio streams received at the decoders.

Cooper has been cited by the Examiner for teaching a selection circuit that passes an input signal as a reference signal when the reference signal has encountered an error (i.e., the reference signal is missing). The Examiner states that the combination of Shuholm with Cooper discloses a selection mechanism that selects an error free signal.

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Watanabe has been cited for teaching an integrated circuit that uses a two mode selector that selects either a second clocking signal or allows a first clocking signal to be applied redundantly.

Claim 1 recites, *inter alia*, "...wherein said reference select circuit: (1) passes a first signal applied to said first reference input to said at least one router component as a first reference signal and a second signal applied to said second reference input to said at least one router component as a second reference signal in response to determining that said first and second signals are error-free..."

By the Examiner's own admission, Shuholm does not teach passing one reference signal in lieu of another. The Examiner has analogized the source inputs, AES 1/2 and AES 3/4 of Shuholm as the first and second reference inputs of the claimed invention. In fact, Shuholm does not discuss reference signals at all. For purposes of this discussion, applicant reproduces the entire detailed description of Shuholm to prevent any further misinterpretation of the same.

Referring now to FIG. 4 a digital audio receiver 10 with multi-channel swapping capabilities receives two or more AES streams. Each AES stream goes through respective decoders 12, 13 which extract the respective clock and audio data (left and right channel samples). The extracted clocks are used to write the audio data from each AES stream to respective synchronizing FIFOs 14, 16, 15, 17. For this example there are four FIFOs 14, 16, 15, 17, one for each channel of audio data from the two AES streams shown. When the channel data are read out of the FIFOs 14, 16, 15, 17 under control of the system clocks 18, they are input to selectors 20, 22. The selectors 20, 22 assign the channel data from the FIFOs 14, 16, 15, 17 to either output stream and to either position within the selected output stream. The output streams from the receiver 10 are then input to a conventional matrix and formatted as shown in FIG. 3. The result is that input streams AES1/2 and AES3/4 may be read out as AES3/2 and AES 1/4 or any other combination depending upon a user's input to the selectors 20, 22. The receiver 10 may be implemented using digital logic, such as is found in a field-programmable gate array (FPGA).

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Thus the present invention provides a digital audio receiver with multi-channel swapping capabilities by receiving at least two AES streams, breaking them into the component channels (left and right) and selecting at the output which two channels make up the at least two AES output streams for input to a conventional matrix in a router.

Shuholm relates to a digital audio receiver with multi-channel swapping capabilities. This is not analogous to a broadcast router that utilizes two (2) reference signal inputs, in addition to the inputs for the input signals. The two inputs (or AES streams), upon receipt, are broken up into component channels (left and right) and at the output a selection is made as to which two channels make up at least the two AES output streams for input into a conventional matrix router.

First, the two AES source inputs of Shuholm are not reference inputs.

Applicant's router, as shown, includes one or more data inputs 143 (see paragraph 0017), and two separate and distinct reference inputs 146 and 148. Thus, since applicant's device includes separate data inputs, the Examiner cannot simply state that the data inputs of Shuholm are analogous to applicant's reference inputs 146 and 148 when the disclosure of Shuholm fails to support the same.

Second, applicant's claim recites "a reference select circuit coupled to said first and second reference inputs ...". Shuholm very specifically teaches that the selector circuits 20 and 22 are not connected to the AES source inputs, but rather are connected to the outputs of the FIFOs (buffers) 14, 15, 16 and 17. The FIFOs receive the output from the AES decoders 12 and 13. Thus, it is clear that Shuholm has not contemplated two reference inputs, as set forth in the claimed invention.

Cooper has been cited for teaching a selection circuit that passes an input signal as a reference signal when the reference signal has encountered an error. By combining the teachings of Cooper with those of Shuholm, the result would at most be one of the AES input streams of Shuholm being used as reference signal in the event a reference signal in Cooper is missing. This is completely contrary to the claimed invention for at least two reasons.

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First, even in such a substitution, there is still only one reference signal. In contrast, we recite two reference signals. Claim 1 recites, for example:

"... wherein said reference select circuit: (1) passes a first signal applied to said first reference input to said at least one router component as a first reference signal and a second signal applied to said second reference input to said at least one router component as a second reference signal in response to determining that said first and second signals are error-free ..." (claim 1, underlining added).

Second, the substitution of the cited art does merely uses an input stream as a reference signal. In contrast, we use an input reference signal as two reference signals. Claim 1 recites, for example:

"... wherein said reference select circuit ... (2) passes said first signal to said at least one router component as said first reference signal and as said second reference signal in response to determining that said first signal is error-free and said second signal is not error-free" (claim 1, underlining added).

Watanabe's shows the use of an external clock different from an internal clock as a reference clock depending on a selector 15, whose position is dependent on the mode selection signal supplied externally (See paragraph 0037). The additional external clock of Watanabe does not cure the deficiency in the combined teachings of Shuholm with Cooper. The asserted combination still has only one reference signal. Nowhere in teachings of Shuholm, Cooper or Watanabe taken singly or in any combination is the concept of passing two distinct reference signals when the two reference signals at two separate reference inputs are error-free.

In view of the above, applicant respectfully requests reconsideration and withdrawal of the rejection of independent claim 1 in its current form.

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Claims 3 and 4 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Shuholm in view of Cooper and Watanabe as applied to claim 1, in further view of Lydon et al. (US Patent No. 6,680,939). Claims 3 and 4 depend from claim 1. The cited portions of Lydon fail to cure, and are not cited to cure, the deficiencies discussed above in the combination of Shuholm, Cooper, and Watanabe. Accordingly, for at least the reasons cited above, claims 3 and 4 are believed to be patentably distinct from the combined teachings of the references.

Claims 5 and 13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Lydon, in view of Shuholm and Watanabe.

Lydon is directed to an expandable router that is adapted to route several different data streams from its input terminals to its output terminals (see Lydon, Abstract). Nowhere does Lydon disclose manipulating reference signals in any way. Furthermore, Lydon also fails to disclose or remotely suggest determining whether signals are "error-free." As explained and shown above, Shuholm does not disclose or suggest the use of two reference inputs. In fact, Shuholm does not disclose or suggest reference inputs of any kind.

Claim 5 recites, *inter alia*: "...a second reference input coupled to said input side of said router matrix, said second reference input configured for selective application of either a second reference signal or a redundancy of said first reference signal thereto."

Lydon teaches the use of N1 signal input terminals and M1 signal output terminals. Thus, a combination of the teachings of Lydon with the two AES inputs of Shuholm clearly fails to disclose, or remotely suggest, the concept of "a second reference input configured for selective application of either a second reference or a redundancy of said first reference signal" (claim 5).

The teachings of Watanabe fail to disclose or suggest two separate and distinct reference inputs, and therefore the combined teachings of Lydon, Shuholm and Watanabe clearly fail to render obvious independent claim 5. Claim 13 is dependent on claim 5 and for at least the reasons cite above is believed to be patentably distinct from the combined teachings of Lydon, Shuholm and Watanabe.

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Claims 6 and 7 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Lydon in view of Shuholm in further view of Donak et al. (U.S. Patent No. 6,330,316) (hereinafter 'Donak').

Claims 6 and 7 depend on claim 5 and include the feature of "a second reference input configured for selective application of either a second reference signal or a redundancy of said first reference signal thereto." As discussed above, Lydon and Shuholm fail to disclose this feature or render this feature obvious. In addition, Donak also fails to disclose this feature or render this feature obvious.

Donak is directed to a method and system for determining whether to route a telephone call over a standard telephone network or an unreliable network, such as the Internet, by measuring the quality of service levels on the unreliable network. Nowhere does Donak disclose employing reference signals. Furthermore, Donak certainly fails to disclose or remotely suggest "a second reference input configured for selective application of either a second reference signal or a redundancy of said first reference signal thereto," as included in claims 6 and 7.

Accordingly, claims 6 and 7 are believed to be patentable over Lydon, Shuholm and Donak, taken singly or in any combination for at least the reasons discussed above.

Claims 8 and 15 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Shuholm in view of Watanabe.

Claim 8 recites, *inter alia* (emphasis added):

providing a broadcast router having first and second reference inputs;
applying a first reference signal to said first reference input;
if a user desires that said broadcast router operate with redundant reference signals, applying said first reference signal to said second reference input; and
if said user desires that said broadcast router operate with multiple reference signals, applying a second reference signal to said second reference input.

Shuholm fails to disclose or render obvious the idea of providing a broadcast router having first and second reference inputs. This alone overcomes this rejection. Notwithstanding the foregoing, Shuholm further fails to disclose the concept of selective application of independent or redundant reference signals at reference signal inputs. That

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is because Shuholm does not discuss or refer to reference signals at all during the processing of the two AES stream inputs.

Watanabe does not cure the deficiencies of Shuholm, simply because the use of an external clock rather than an internal clock by the device of Shuholm fails to render obvious the idea of providing a broadcast router having first and second reference inputs. Furthermore, Watanabe's selection of the external clock signal is based on a mode selection signal, and not based on a determination to use redundant or multiple reference signals. In fact, the combined teachings of Shuholm with Watanabe clearly fail to disclose or even remotely suggest the idea of "...applying a second reference signal to said second reference input" when the broadcast router is to be operated with multiple reference signals.

Accordingly, claims 8 and 15 is believed to be patentable over Shuholm and Watanabe, taken singly or in combination for at least the reasons discussed above. Withdrawal of the rejection is respectfully requested.

Claims 9 and 10 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Shuholm and Watanabe in further view of Cooper. Claims 9 and 10 depend ultimately from claim 8, and for at least the reasons cited above, are believed to be patentably distinct from the combined teachings of the references of Shuholm, Watanabe, and Cooper.

Claim 12 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Shuholm in view of Cooper and Watanabe, in further view of Bytheway ("Is your plant infrastructure ..."). Claim 12 is dependent on claim 1. As discussed above, claim 1 is patentably distinct from the combined teachings of Shuholm, Cooper, and Watanabe. The cited portions of Bytheway are not cited to cure, and do not cure, the deficiencies of the combination of Shuholm, Cooper, and Watanabe. Accordingly, claim 12 is believed to be patentably distinct from the asserted combination including Bytheway.

Claim 14 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Lydon in view of Shuholm and Watanabe, in further view of Bytheway. Claim 16 stands

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rejected under 35 U.S.C. §103(a) as being unpatentable over Shuholm in view of Watanabe, in further view of Bytheway. Claim 14 depends from independent claim 5, and claim 16 depends from independent claim 8. The cited portions of Bytheway are not cited to cure, and do not cure, the deficiencies discussed with respect to the rejections of claims 5 and 8. Accordingly, for at least the reasons cited above with respect to independent claims 5 and 8, applicant believes claims 14 and 16 are patentably distinct from the teachings of the new combined references.

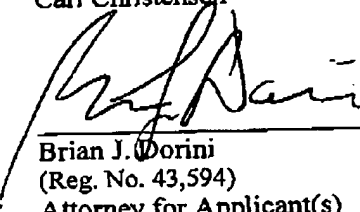
Accordingly, it is respectfully submitted that all pending claims are allowable over the cited references.

In view of the foregoing, Applicant respectfully requests that the rejections of the claims set forth in the Office Action of April 21, 2008 be withdrawn, that pending claims 1-16 be allowed, and that the case proceed to early issuance of Letters Patent in due course.

It is believed that no additional fees or charges are currently due. However, in the event that any additional fees or charges are required at this time in connection with the application, they may be charged to applicant's representatives Deposit Account No. 07-0832.

Respectfully submitted,

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